Q.P. Code: 18EC0402 **R18**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Regular Examinations Nov/Dec 2019

DIGITAL SYSTEM DESIGN

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 60

PART-A

(Answer all the Questions **5 x 2 = 10** Marks)

1	**a**	Find 10's complement of given decimal numbers X = 52324 and Y =2421.	**2M**
	b	Implement a Full Adder using Half Adders.	**2M**
	c	Write the difference between Latch and Flip-flop.	**2M**
	d	What are the advantages of PLDs.	**2M**
	e	Define FSM.	**2M**

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	**a**	State and prove De Morgan's theorem.	**4M**
	b	Perform the following using BCD arithmetic. i) $(79)_{10} + (177)_{10}$ ii) $(481)_{10} + (178)_{10}$	**6M**
		OR	
3	**a**	Express the Boolean function, F= A+B'C as a sum of minterms.	**4M**
	b	Obtain the Dual and complement for the following Boolean expressions. i) F=AB+A (B+C) + B' (B+D) ii) F=A+B+A'B'C iii)F=A'B+A'BC'+A'BCD+A'BC'D'E	**6M**

UNIT-II

4	**a**	Simplify $F(A,B,C,D) = \sum (4,5,6,7,12,13,14) + d(1,9,11,15)$ using K-map.	**5M**
	b	Simplify the following Boolean function for minimal SOP form using K-map. i) $F(A, B, C, D) = \Sigma (0,1,2,5,8,9,10)$ ii) $F(A, B, C, D) = \pi(1,3,5,7,12,13,14,15)$.	**5M**
		OR	
5	**a**	Define Decoder. Design & implement a 3 to 8 line Decoder**.**	**5M**
	b	Design & implement a 4-bit binary Adder/subtractor.	**5M**

UNIT-III

6	**a**	Draw the logic diagram of a JK – flip flop and explain its operation.	**5M**
	b	Explain the operation of an SR Flip Flop using excitation table. Give its Truth Table and Characteristic Equation.	**5M**
		OR	
7	**a**	Explain the operation of Pseudo Random Binary Sequence Generator with a neat diagram.	**5M**
	b	Design a 4-bit Synchronous Up counter using JK flip-flops.	**5M**

UNIT-IV

8	**a**	Perform the analysis of standard TTL NAND gate and give its characteristics.	**6M**
	b	Give the comparison of different CMOS Logic families.	**4M**
		OR	
9	**a**	Implement the following functions using PLA, $F(w,x,y)=\sum m(3,5,6,7)$	**5M**
	b	Explain the architecture of PLA.	**5M**

UNIT-V

10	**a**	Explain various Data Types in VHDL.	**5M**
	b	Write a VHDL program for a 4X1 MUX.	**5M**
		OR	
11	**a**	Write a VHDL program for a 3 to 8 line Decoder.	**5M**
	b	Explain about Simulation and Synthesis processes in VHDL.	**5M**

END